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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/288,263	04/08/1999	HIROYUKI WAKI	NAK1-BG55	7236

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EXAMINER

LAFORGIA, CHRISTIAN A

ART UNIT	PAPER NUMBER
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2155

DATE MAILED: 02/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/288,263

Applicant(s)

WAKI ET AL.

Examiner

Christian La Forgia

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 January 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 29-31 and 39-51 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 29-31 and 39-51 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 January 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>4</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The amendment filed on 17 January 2003 is noted and made of record.
2. Claims 29 through 31 and 39 through 51 are presented for examination.

Drawings

3. The corrected or substitute drawings were received on 17 January 2003. These drawings are approved.
4. The Patent and Trademark Office no longer makes drawing changes. See 1017 O.G. 4.

It is applicant's responsibility to ensure that the drawings are corrected. Corrections must be made in accordance with the instructions below.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. **Correction of Informalities -- 37 CFR 1.85**

New corrected drawings must be filed with the changes incorporated therein. Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. **Corrections other than Informalities Noted by Draftsperson on form PTO-948.**

All changes to the drawings, other than informalities noted by the Draftsperson, **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes.

Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.185(a). Failure to take corrective action within the set (or extended) period will result in **ABANDONMENT** of the application.

Response to Amendment

5. The amendment filed on 17 January 2003 under 37 CFR 1.131 has been considered but is ineffective to overcome the Tremblay reference.
6. The amendment filed on 17 January 2003 under 37 CFR 1.131 has been considered but is ineffective to overcome the Wahbe reference.

Response to Arguments

7. Applicant's arguments filed 17 January 2003 have been fully considered but they are not persuasive.
8. In response to the Applicant's assertion that Tremblay fails to teach "storing each virtual machine instruction in the virtual machine instruction sequence associated with different succeeding instruction information, the succeeding instruction information for a given virtual machine instruction indicating a change in a storage state of data in a stack due to execution of a virtual machine instruction executed after the given virtual machine instruction," the Examiner believes that Tremblay teaches this claim limitation. The Examiner directs the Applicant's attention to column 8, line 61 to column 9, line 42, specifically Tremblay's discussion of incoming arguments. The Examiner particularly refers to column 9, lines 31 to 40, where Tremblay teaches "Like the object reference, the incoming arguments are pushed onto stack 400 by JAVA compiler generated instructions and may be accessed as local variables. JAVA compiler JAVAC (see Figure 2) statically generates a list of arguments for current method 410 (Figure 4a) and hardware processor 1000 determines the number of arguments from the list.

When the object reference is present in the frame for a non-static method invocation, the first argument is accessible as local variable one.”

9. Furthermore, in response to the Applicant’s teachings of stack management, the Examiner acknowledges this teaching, and believes it to be a common and accepted definition in the art. Additionally, Tremblay makes reference to a similar method of stack management as disclosed by the Applicant. Tremblay gives an in depth explanation of how the Virtual Machine accesses the stack in column 9, line 57 to column 10, line 23.
10. In response to the Applicant’s arguments that Tremblay does not teach “each branch instruction stored in the branch instruction area designating a branch destination using an identifier stored in one of the identifier areas,” the Examiner asserts that Tremblay teaches this claim limitation. The Examiner again makes reference to Figure 1, particularly that which is labeled as part number 133 *Branch Predictor*. Furthermore, the branch instruction area is discussed in Tremblay in column 15, lines 12 to 25.
11. In response to the Applicant’s argument that Wahbe does not teach that the basic blocks are divided by the virtual machine, but instead divided by the compiler, the Examiner calls attention to Figures 4 and 7. In Figure 4, the Examiner directs the Applicant to Steps 427, 430, and 434, it is here that Wahbe teaches the dividing of the program into basic blocks. Wahbe further goes on in Figure 7, step 731 to teach that the division is done in the step of compiling. Wahbe teaches this in column 7, line 66 to column 8, line 16 and column 16, line 28 to column 17, line 62. In response to Applicant’s assertion on page 10 of the amendment filed on 17 January 2003, that the “virtual machine does not have to divide the virtual machine codes into the basic blocks as in Wahbe ‘618,” the Examiner asserts that Wahbe does not always divide

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code into the basic blocks, he only breaks code into basic blocks in order to optimize the program code. Wahbe teaches this in Figure 4, step 427, the step request "Are Program Optimizations Required?"

12. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

13. See further 35 USC § 102 and 35 USC § 103 rejections that follow.

Claim Rejections - 35 USC § 102

14. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

15. Claims 29, 30, and 45 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 6,021,469 to Tremblay et al., (hereinafter Tremblay).

16. As per claim 29, Tremblay teaches a storage method used by instruction storing means that stores a virtual machine instruction sequence generated by compiler to be executed by a virtual machine, having a stack architecture (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57),

17. the storage method being characterized by storing each virtual machine instruction in the virtual machine instruction sequence associated with different succeeding instruction information, the succeeding instruction information for a given virtual machine instruction indicating a change in a storage state of data in a stack due to execution of a virtual machine

instruction executed after the given virtual machine instruction (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57).

18. Regarding claim 30, Tremblay teaches a storage method used by instruction storing means that stores a virtual machine instruction sequence generated by compiler to be executed by a virtual machine (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57),

19. wherein the storage method results in:

20. the instruction storing means being a plurality of instruction blocks that constitute the virtual machine instruction sequence, the instruction blocks corresponding to basic blocks (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57);

21. the instruction blocks including:

an identifier area for storing an identifier that specifies a start position of the instruction block in the instruction storing means (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57);

a non-branch instruction area for storing non-branch instructions belonging to a corresponding basic block (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57);

a branch instruction area for storing at least one branch instruction belonging to the corresponding basic block (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57); and

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22. each branch instruction stored in the branch instruction area designating a branch destination using an identifier stored in one of the identifier areas (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57).
23. Regarding claim 45, Tremblay teaches a computer-readable recording medium for recording a program that enables a computer to carry out the storage method (Figures 1 & 3; column 5, line 36 to column 6, line 54; column 7, lines 51-63).
24. Claims 39 through 41, and 46 through 48 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent No. 6,151,618 to Wahbe et al., (hereinafter Wahbe).
25. Regarding claim 39, Wahbe teaches a storage method used by instruction storing means that stores a virtual machine instruction sequence generated by compiler to be executed by a virtual machine,
26. wherein the storage method results in:
27. the instruction storing means being a plurality of instruction blocks that constitute the virtual machine instruction sequence, the instruction blocks corresponding to basic blocks (Figures 4, 6, & 7; column 11, line 58 to column 12, line 13);
28. the instruction blocks each including:
- an identifier area for storing an identifier that specifies a start position of the instruction block in the instruction storing means (Figures 4, 6, & 7; column 12, lines 14-30);

a non-branch instruction area for storing non-branch instructions belonging to the corresponding basic block (Figures 4, 6, & 7; column 11, line 58 to column 12, line 13); and,

a branch instruction area for storing at least one branch instruction belonging to the corresponding basic block (Figures 4, 6, & 7; column 11, line 58 to column 12, line 13).

29. As per claim 40, Wahbe teaches wherein the identifier of the instruction block is address related information in the virtual machine instruction sequence (Figures 4, 6, & 7; column 12, lines 14-30).

30. As per claim 41, Wahbe teaches wherein the address related information is one of absolute address, relative address, and offset address (Figures 4, 6, & 7; column 12, lines 14-30).

31. As per claims 46 through 48, Wahbe teaches a computer-readable recording medium for recording a program that enables a computer to carry out the storage method (Figures 1 through 3; column 5, line 20 to column 7, line 12).

Claim Rejections - 35 USC § 103

32. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

33. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tremblay in view of United States Patent No. 4,177,514 to Rupp.

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34. As per claim 31, Tremblay teaches a computer-readable recording medium that stores a program to have a computer function as a virtual machine with a stack architecture (Figures 1, 2, & 4A; column 5, line 36 to column 6, line 28; column 7, lines 30-57),
35. wherein the virtual machine comprises:
36. instruction storing means for storing a virtual machine instruction sequence and a plurality of sets of succeeding instruction information, wherein each virtual machine instruction in the virtual machine instruction sequence is associated with a set of succeeding instruction information that indicates a change in a storage state of the data in the stack means due to an execution of a virtual machine instruction executed after the associated virtual machine instruction (Figure 1; column 7, lines 30-57);
37. read means for reading a virtual machine instruction and an associated set of succeeding instruction information from the instruction storing means (Figure 1; column 7, lines 30-57); and,
38. decoding executing means for specifying and executing operations corresponding to a combination of the read virtual machine instruction and the read set of succeeding instruction information (Figure 1; column 5, line 36 to column 6, line 28; column 7, lines 30-57).
39. Tremblay does not teach a stack means for temporarily storing data in a last-in first-out format.
40. Rupp teaches a stack means for temporarily storing data in a last-in first-out format (column 53, line 63 to column 54, line 7). Therefore, it would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the stack management

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means of Rupp with the system of Tremblay, because it would enable a quick and efficient way to manage the stack.

41. Claims 42 through 44 and 49 through 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wahbe in view of Tremblay.

42. As per 42, Wahbe does not teach wherein whether each virtual machine instruction is positioned at a start position of the basic block is indicated by an address in the virtual machine instruction sequence to which the virtual machine instruction is allocated;

43. a virtual machine instruction at the start position of the basic block being allocated to a specific address in the virtual machine instruction sequence, and

44. a virtual machine instruction at other than the start position of the basic block being allocated to an address other than the specific address.

45. Tremblay teaches wherein whether each virtual machine instruction is positioned at a start position of the basic block is indicated by an address in the virtual machine instruction sequence to which the virtual machine instruction is allocated (Figures 4A & 4B; column 19, line 1 to column 21, line 5);

46. a virtual machine instruction at the start position of the basic block being allocated to a specific address in the virtual machine instruction sequence (Figures 4A & 4B; column 19, line 1 to column 21, line 5), and

47. a virtual machine instruction at other than the start position of the basic block being allocated to an address other than the specific address (Figures 4A & 4B; column 19, line 1 to column 21, line 5). It would have been obvious to one with ordinary skill in the art at the time

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the invention was made to include the addressing of Tremblay with the system of Wahbe, because it would create a quicker and more efficient method to access the next sequence of data.

48. As per claim 43, Wahbe teaches an identifying unit for storing identification information which indicates if the virtual machine instruction is positioned at a start position of the basic block (Figures 4, 6, & 7; column 12, lines 14-30). Wahbe does not teach an operation specifying unit for specifying an operation to be executed by the virtual machine.

49. Tremblay teaches an operation specifying unit for specifying an operation to be executed by the virtual machine (Figures 1 & 2; column 5, line 36 to column 6, line 54). It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the addressing of Tremblay with the system of Wahbe, because it would create a quicker and more efficient method to access the next sequence of data.

50. As per claim 44, Wahbe teaches the basic blocks (Figures 4, 6, & 7; column 11, line 58 to column 12, line 13); and,

51. identification tags, each designates an address related information of the virtual machine instruction at a start position of the basic block; attachment of the tag indicating if the virtual machine instruction corresponding to the identification tag is positioned at the start position of the basic block (Figures 4, 6, & 7; column 12, lines 14-30).

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52. As per claims 49 through 51, Wahbe teaches a computer-readable recording medium for recording a program that enables a computer to carry out the storage method (Figures 1 through 3; column 5, line 20 to column 7, line 12).

Conclusion

53. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

54. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

55. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian La Forgia whose telephone number is (703) 305-7704. The examiner can normally be reached on Monday thru Thursday 7-5.


56. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (703) 305-9648. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7240 for regular communications and (703) 746-7239 for After Final communications.

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57. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Christian La Forgia
Patent Examiner
Art Unit 2155

clf
February 9, 2003


AYAZ SHEIKH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100